WHAT IS CLAIMED IS

1. A method of fabricating a semiconductor integrated circuit device, comprising the steps of:

forming a device isolation structure on a surface of a semiconductor substrate so as to define at least a first active region, a second active region and a third active region,

introducing an impurity element that suppresses oxidation of said semiconductor substrate into said first active region;

applying a thermal oxidation process to said surface of said semiconductor substrate to form a first insulation film so as to cover said semiconductor substrate surface in said first active region with a first thickness and a second insulation film so as to cover said semiconductor substrate surface in said second and third active regions with a second thickness;

forming an oxidation-resistant film on said surface of said semiconductor substrate so as to cover at least said first active region and said second active region and said third active region;

exposing said surface of said semiconductor substrate by removing said oxidation-resistant film and said second insulation film from said third active region while leaving said oxidation-resistant film on said first and second active regions;

applying a thermal oxidation process to said semiconductor substrate to form a third thermal oxide film on said third active region with a third thickness and to increase a thickness of said second thermal oxide film simultaneously.

2. A method of fabricating a semiconductor integrated circuit, comprising the steps of:

forming a device isolation structure on a surface of a semiconductor substrate so as to define at least a non-volatile memory cell region and a first active region and a second active region;

applying a thermal oxidation process to said semiconductor substrate to form a tunneling oxide film on said surface of said semiconductor substrate so as to cover said non-volatile memory cell region and said first active region and said second active region;

depositing a silicon film and an oxidation-resistant insulation film including a nitride film consecutively on said semiconductor substrate so as to include at least said non-volatile memory cell region and said first active region and said second active region;

exposing said surface of said semiconductor substrate selectively in said first active region;

applying a thermal oxidation process to said semiconductor substrate so as to form a first insulation film on said surface of said semiconductor substrate in said first region;

exposing said surface of said semiconductor substrate selectively in said second active region; and

applying a thermal oxidation process to said semiconductor substrate so as to form a second insulation film in said second region.

3. A method of fabricating a semiconductor integrated circuit, comprising the steps of:

forming a device isolation region on a surface of a semiconductor substrate so as to define

at least a non-volatile memory cell region, a first active region and a second active region,

applying a thermal oxidation process to said semiconductor substrate to form a tunneling oxide film so as to cover at least said non-volatile memory cell region and said first active region and said second active region;

depositing a silicon film on said semiconductor substrate so as to include at least said flash memory cell region and said first and second active regions;

removing said silicon film selectively from said first and second active regions;

depositing an oxidation-resistant insulation film on said semiconductor substrate so as to cover at least said non-volatile memory cell region and said first active region and said second active region;

exposing said surface of said semiconductor substrate by removing said oxidation-resistant insulation film selectively from said first active region;

applying a thermal oxidation process to said semiconductor substrate while using said oxidation-resistant insulation film remaining on said semiconductor substrate as an anti-oxidation mask, to form a first insulation film so as to cover said surface of said semiconductor substrate in said first active region;

removing said oxidation-resistant insulation film selectively in said second active region to expose said surface of said semiconductor substrate;

applying a thermal oxidation process to said semiconductor substrate while using said oxidation-resistant insulation film remaining on said semiconductor substrate as an anti-oxidation mask to form a second insulation film in said second active region so as to cover said surface of said

semiconductor substrate.

4. A method of fabricating a semiconductor device, comprising the steps of:

forming a device isolation structure on a surface of a semiconductor substrate so as to define a non-volatile memory cell region and a first active region and a second active region and a third active region;

introducing an impurity element that suppresses oxidation of said semiconductor substrate into said first active region;

applying a thermal oxidation process to said semiconductor substrate to form a tunneling oxide film having a first thickness in said non-volatile memory cell region and in said second and third active regions with a first thickness and a first insulation film in said having a second thickness smaller than said first thickness in said first active region;

depositing a silicon film and an oxidation-resistant film consecutively on said semiconductor substrate so as to include said non-volatile memory cell region and said first through third active regions;

removing said oxidation-resistant film selectively in said second active region to expose said surface of said semiconductor substrate;

forming a second insulation film in said second active region so as to cover said surface of said semiconductor substrate in said second region by applying a thermal oxidation process to said semiconductor substrate while using said oxidation-resistant insulation film remaining on said semiconductor substrate as an anti-oxidation mask;

exposing said surface of said semiconductor substrate in said third active region by selectively removing said oxidation-resistant insulation film therefrom;

applying a thermal oxidation process to said semiconductor substrate while using said oxidation-resistant insulation film as a mask to form a third insulation film in said third active region so as to cover said surface of said semiconductor substrate.

5. A method of fabricating a semiconductor device, comprising the steps of:

forming a device isolation structure on a surface of a semiconductor substrate so as to define a non-volatile memory cell region, a first active region, a second active region and a third active region;

introducing an impurity element suppressing oxidation into said first active region;

applying a thermal oxidation process to said semiconductor substrate to form a tunneling oxide film having a first thickness in said non-volatile memory cell region and in said second and third active regions and a first insulation film having second thickness smaller than said first thickness in said first active region;

depositing a first silicon film and an oxidation-resistant insulation film consecutively on said semiconductor substrate so as to cover said tunneling oxide film in each of said non-volatile memory cell region and in said second and third active regions and so as to cover said first insulation film in said first active region;

exposing said surface of said semiconductor

substrate in said second active region by selectively removing said oxidation-resistant insulation film;

applying a thermal oxidation process to said semiconductor substrate while using said oxidation-resistant insulation film remaining on said semiconductor substrate as a mask to form a second insulation film so as to cover said surface of said semiconductor substrate in said second active region;

exposing said surface of said semiconductor substrate by selectively removing said oxidation-resistant insulation film from said third active region;

applying a thermal oxidation process to said semiconductor substrate while using said oxidation-resistant insulation film remaining on said semiconductor substrate as a mask to form a third thermal oxide film so as to cover said surface of said semiconductor substrate in said third active region;

removing said oxidation-resistant insulation film selectively from said first active region; and

depositing a second silicon film on said semiconductor substrate so as to cover said non-volatile memory cell region and said first through third active regions.

6. A method of fabricating a semiconductor integrated circuit, comprising the steps of:

forming a device isolation structure on a surface of a semiconductor substrate so as to define a non-volatile memory cell region, a first active region, a second active region and a third active region;

introducing an impurity element suppressing oxidation into said first active region;

applying a thermal oxidation process to said semiconductor substrate to form a tunneling oxide film having a first thickness in said non-volatile memory cell region and in said second and third active regions and a first insulation film having a second thickness smaller than said first thickness in said first active region;

depositing a first silicon film and an oxidation-resistant insulation film consecutively on said semiconductor substrate so as to include said non-volatile memory cell region and said first through third active regions;

exposing said surface of said semiconductor substrate by removing said oxidation-resistant insulation film selectively from said second active region;

applying a thermal oxidation process to said semiconductor substrate while using said oxidation-resistant insulation film remaining on said semiconductor substrate as an anti-oxidation mask to form a second insulation film in said second active region so as to cover said surface of said semiconductor substrate;

exposing said surface of said semiconductor substrate by removing said oxidation-resistant insulation film selectively from said third active region;

applying a thermal oxidation process to said semiconductor substrate while using said oxidation-resistant insulation film remaining on said semiconductor substrate as a mask to form a third insulation film on said third active region so as to cover said surface of said semiconductor substrate;

depositing a second silicon film on said semiconductor substrate so as to include said non-volatile memory cell region and said first through third active regions; and

removing said second silicon film and said oxidation-resistant insulation film from said first active region selectively.

7. A method as claimed in claim 6,further comprising the step of depositing a third silicon film on said semiconductor substrate so as to include said non-volatile memory cell region and said first through third active regions.

8. A method of fabricating a semiconductor integrated circuit device, comprising the steps of:

forming a device isolation structure on a surface of a semiconductor substrate so as to define a non-volatile memory cell region, a first active region, a second active region and a third active region;

applying a thermal oxidation process to said semiconductor substrate to form a tunneling oxide film in said non-volatile memory cell region and in said second and third active regions with a first thickness and a first insulation film having a second thickness smaller than said first thickness in said first region;

depositing a first silicon film and an oxidation-resistant insulation film on said semiconductor substrate so as to cover said tunneling oxide film in each of said non-volatile memory cell region and said second and third active regions and so as to cover said first insulation film in said first active region;

exposing said surface of said semiconductor substrate by selectively removing said oxidation-resistant insulation film from said second active region;

applying a thermal oxidation process to said semiconductor substrate while using said oxidation-resistant insulation film as a mask to form a second insulation film in said second active region so as to cover said surface of said semiconductor substrate;

exposing said surface of said semiconductor substrate in said third active region by removing said oxidation-resistant insulation film selectively;

applying a thermal oxidation process to said semiconductor substrate while using said oxidation-resistant insulation film remaining on said semiconductor substrate as an anti-oxidation mask to form a third insulation film in said third active region so as to cover said surface of said semiconductor substrate;

depositing a second silicon film on said semiconductor substrate so as to include said non-volatile memory cell region and said first through third active regions; and

forming a control gate pattern in said non-volatile memory cell region by patterning said second silicon film and simultaneously removing said second silicon film from said first active region.

9. A method of fabricating a semiconductor integrated circuit, comprising the steps of:

forming a device isolation structure on a surface of a semiconductor substrate so as to define a non-volatile memory cell region and a first active region and a second active region and a third active

region;

applying a thermal oxidation process to said semiconductor substrate to form a first insulation film in said non-volatile memory cell region and said first through third active regions;

depositing a first silicon film on said semiconductor substrate so as to include said non-volatile memory cell region and said first through third active regions;

exposing said surface of said semiconductor substrate selectively in said second active region by removing said first silicon film said second active region;

applying a thermal oxidation process to said semiconductor substrate to form a second insulation film inn said second active region so as to cover said surface of said semiconductor substrate in said second active region;

introducing an impurity element suppressing oxidation into said semiconductor substrate in said third active region;

exposing said surface of said semiconductor substrate by removing said first silicon film and said first insulation film selectively from said non-volatile memory cell region and said third active region;

applying a thermal oxidation process to said semiconductor substrate to form a tunneling oxide film so as to cover said surface of said semiconductor substrate in said non-volatile memory cell region and simultaneously a third insulation film so as to cover said surface of said semiconductor substrate in said third active region;

depositing a second silicon film on said semiconductor substrate so as to include said non-volatile memory cell region and said first through third active regions;

forming a gate electrode in said non-volatile memory cell region by patterning said second silicon film and simultaneously removing said silicon film from said first active region.

10. A method of fabricating a semiconductor integrated circuit, comprising the steps of:

forming a device isolation structure on a semiconductor substrate so as to define a non-volatile memory cell region and first through third active regions;

forming a first oxidation film, a nitride film and a second oxide film on each of said non-volatile memory cell region and said first through third active regions so as to cover said surface of said semiconductor substrate;

exposing said surface of said semiconductor substrate by selectively removing said first oxide film, said nitride film and said second oxide film from said first active region;

applying a thermal oxidation process to said semiconductor substrate to form a first insulation film on said surface of said semiconductor substrate in said first active region;

exposing said surface of said semiconductor substrate by selectively removing said first oxide film, said nitride film and said second oxide film from said second active region;

applying a thermal oxidation process to said semiconductor substrate to form a second insulation film on said surface of said semiconductor substrate in said second active region;

exposing said surface of said semiconductor substrate by selectively removing said first oxide

film, said nitride film and said second oxide film from said third active region; and

applying a thermal oxidation process to said semiconductor substrate to form a third insulation film in said third active region.

11. A method of fabricating a semiconductor integrated circuit, comprising the steps of:

forming a device isolation structure on a semiconductor substrate so as to define a non-volatile memory cell region and first through third active regions;

forming a first oxide film, a nitride film and a second oxide film on each of said non-volatile memory cell region and said first through third active regions so as to cover a surface of said semiconductor substrate;

exposing said surface of said semiconductor substrate by removing said first oxide film, said nitride film and said second oxide film selectively from said first active region;

applying a thermal oxidation process to said semiconductor substrate, said first oxide film, said nitride film and said second oxide film to form a first insulation film on said surface of said semiconductor substrate in said first active reigon;

exposing said surface of said semiconductor substrate by removing said first oxide film, said nitride film and said second oxide film selectively from said second active region;

applying a thermal oxidation process to said semiconductor substrate, said first oxide film, said nitride film and said second oxide film to form a second insulation film on said surface of said

semiconductor substrate in said second active region;

exposing said surface of said semiconductor substrate by selectively removing said first oxide film, said nitride film and said second oxide film from said third active region;

applying a thermal oxidation process to said semiconductor substrate, said first oxide film, said nitride film and said second oxide film to form a third insulation film on said surface of said semiconductor substrate in said third active region.

12. A method as claimed in claim 1, wherein said oxidation-resistant insulation film has a structure in which a nitride film is sandwiched by a pair of oxide films.

13. A method as claimed in claim 1, wherein one of said first and second insulation films has a structure in which a plurality of insulation films are stacked.

14. A method as claimed in claim 4, wherein one of said first through third insulation films has a structure in which a plurality of insulation films are stacked.

15. A method as claimed in claim 1, wherein said impurity element is nitrogen.

16. A semiconductor integrated circuit, comprising:

a semiconductor substrate;

a non-volatile memory formed in a memory cell region of said semiconductor substrate;

a first MOS transistor formed on a first device region of said semiconductor substrate, said first MOS transistor having a first gate insulation film of first thickness and a first gate electrode;

a second MOS transistor formed on a second device region of said semiconductor substrate, said second MOS transistor having a second gate oxide film of second thickness and a second gate electrode; and

a third MOS transistor formed on a third device region of said semiconductor substrate, said third MOS transistor having a third gate insulation film of third thickness and a third gate electrode;

said first thickness being smaller than said second thickness, said second thickness being smaller than said third thickness,

said first through third gate electrodes having a substantially identical height.

17. A semiconductor integrated circuit as claimed in claim 16, wherein said first and third gate electrodes have a structure in which a second silicon film is stacked on a first silicon film, said second gate electrode has a structure in which said second

silicon film is stacked on a third silicon film, and wherein said non-volatile memory is formed of a floating gate electrode formed of said third silicon film and a control gate electrode formed on said floating gate electrode via an insulation film and having a structure in which said first silicon film and said second silicon film are stacked consecutively.

18. A semiconductor integrated circuit as claimed in claim 16, wherein said non-volatile memory comprises a floating gate electrode of a first silicon film and a control gate electrode of a second silicon film formed on said floating gate electrode via an insulation film, said first and third gate electrodes being formed of said second silicon film, said second gate electrodes being formed of said first silicon film.